Single-Event Upset Test Results for the Xilinx XQ1701L PROM

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Abstract

Three types of heavy-ion upsets occurred in an advanced FPGA-configuration PROM: (1) address errors, (2) premature end-of-program signals, and (3) functional interrupt. The threshold LETs were near 5 MeV-cm^2/mg. Latchup was also measured above a higher threshold LET of 55. These SEEs limit viable space applications for this device.

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Introduction

Programmable logic devices are frequently used in space applications because of the ease of reconfiguration which significantly lowers overall cost. Earlier work has been done to investigate the effects of radiation on some of these technologies [1-6], most of which used antifuse technology for programming. The technology used by Xilinx in their SRAM-configurable gate-arrays requires an initial programming sequence on power-up in order to program the gate array. This paper presents test results for an advanced, 3.3-V PROM that is designed to interface with Xilinx FPGAs (field programmable gate arrays) and provide the initialization sequence. This device, the XQ1701L, has a storage capacity of approximately 1-Mb and is fabricated on a bulk substrate. It can be operated in a low-current standby mode as well as in a normal mode.

The XQ1701L is a one-time programmable read only memory with a serial output. It is compatible with the configuration requirements of a number of 3.3-V Xilinx XC4000 and 2.5-V Virtex family SRAM-based FPGAs which are attractive to spacecraft designers. However, the configuration memory that is loaded by the PROM is SEU susceptible [3,4]. The threshold LET was approximately 5 MeV-cm^2/mg for both 5-V and 3.3-V FPGAs.

Xilinx is marketing a number of their FPGAs with a 7 μm epitaxial layer as high reliability, radiation tolerant devices in ceramic packages. The "radiation tolerant" claim is based on (1) no observed SEL, (2) moderate TID levels, (3) moderate SEU LET threshold, and (4) the capability of continuously monitoring the configuration SRAM for upsets. Since re-loading the FPGA takes a large fraction of a second, designs for collecting critical data or controlling expendables require a significant risk mitigation effort. These FPGAs do appear suited to a broad range of other applications, such as sensor and camera controllers.

The PROM is critical for these applications, because any errors in the PROM will cause erroneous configuration of the FPGAs with which it interfaces. The present work is the first heavy ion testing reported for these devices. Unlike the FPGAs, the configuration PROM is not fabricated on an epitaxial substrate; as shown later, the PROM is susceptible to single-event latchup (SEL). The continuous monitoring capability proposed by Xilinx requires checking the SRAM contents against a known good copy, presumably from the PROM. Thus, the various PROM upset phenomena observed will cause malfunctions of configuration monitoring, making spacecraft usage more problematic.

Test Device Properties

Three XQ1701LCC44 (date code 9849) samples in 44-pin VQFP packages were tested, one unprogrammed (s/n: 3848) and two programmed (s/n: 3849 and 3850). Only three pins are used to exercise the devices with a fourth for the serial output and a fifth for output control. Additionally, there are three power pins; the remaining 36 pins have no connection.

The devices were programmed using a Xilinx HW130 programmer. Device 3848 was not recognized by the programmer, necessitating leaving it unprogrammed. A short section of S/N 3849 would not program to the intended pattern, but the test software was modified to ignore the problem. The low programming success rate (one in three) may be indicative of device quality/consistency problems or may be related to the programmer itself which was not calibrated or otherwise checked out immediately prior to this use.

The pattern programmed into the devices was approximately half "ones" and half "zeros"and was designed to permit trapping of selected types of errors. Although this does not correspond to a typical configuration pattern, it provides visibility of selected types of errors during dynamic testing. Additional details will be provided in the full paper.

Approach Used for Radiation Testing

SEU and latchup tests were done at Brookhaven National Laboratory. Properties of the ions that were used are listed in Table 1, below. Because this device has a bulk substrate, ion range is an important consideration.

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†The work described in this paper was carried out by the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration, Code AE. Work funded by the NASA Microelectronics Space Radiation Effects Program (MSREP).

Table 1. Ions Used for SEU Testing

Ion	Energy (MeV)	LET (MeV-cm²/mg)	Range (μm)
F	150	3.2	>100
Cl	210	11.5	81
Ni	260	27	40
Br	290	37	36
I	350	60	31

Dynamic testing was done on these devices during the time that they were exposed to heavy ions. A PCI interface card was used, connected to the device under test with a TTL-differential receiver that could drive fast signals over ribbon cable. Special software was used, containing a dynamic link library to handle I/O routines. The I/O routines were written in Visual C++5 and the user interface routines were written in Visual Basic.

Two different algorithms were used to determine whether the PROM functioned properly. The first algorithm began by resetting the part, and then applying a sequence of clock signals. With this algorithm, no attempt was made to compare the output of the memory. Error detection was based on detection of the end-of-address space output (CEO pin), ensuring that it only provided an output at the end of the proper number of clock cycles. If the CEO output occurred prematurely, that indicated that an error had occurred in the address control logic. The advantage of the first algorithm was ease of execution. It was primarily used in initial evaluations of the device to determine what types of errors and malfunctions occurred.

The second algorithm was more complete, and executed a bit-by-bit comparison of the actual output of the PROM with the contents expected from the initial programming. The bit read position could be dynamically adjusted. The more complex algorithm could detect address failures and individual bit errors.

Functional Test Results

Changes in the internal stored data were not observed in this PROM device. However, errors were observed in the bit stream as well as overall functionality errors. The functionality errors interfered with the quantification of bit-stream upsets.

The first type of functional error occurred in the end-of-pass output signal (EOP) which indicates the end of a read cycle. That signal is of critical importance in applications of the XQ1701 device, and could be detected by both of the test algorithms. The false EOP condition causes the output of the device to "freeze" and any errors that produce an erroneous EOP result will be difficult to recover from in most applications. During SEU tests, a number of EOP errors occurred. Figure 1 shows how the cross section for EOP errors depends on LET. The threshold LET is approximately 10 MeV-cm²/mg. The cross section gradually increases by about two orders of magnitude with increasing LET. EOP errors persist until the part undergoes reset or power cycling.

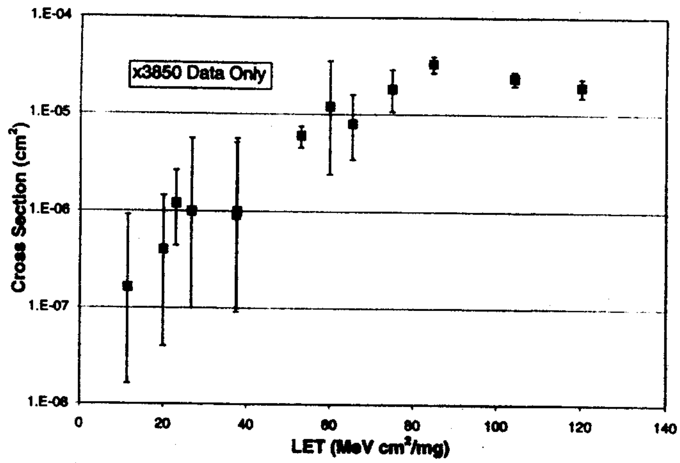

Figure 1. Cross section for end-of-pass errors in the Xilinx XQ1701L PROM.

Address failures were also observed during the SEU tests. The address failures were observed by comparing the actual location of data within the device with the expected location based on the number of data strobe cycles. Figure 2 shows how the cross section for address errors depends on LET. The threshold LET was approximately 5 MeV-cm²/mg. Recovery from address failures required reset or power cycling.

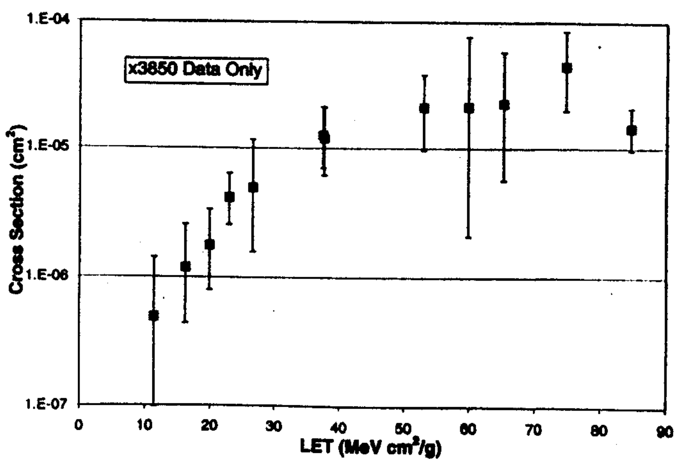

Figure 2. Cross section for address errors in the Xilinx XQ1701L PROM.

Several events were also observed where part functionality was lost, and the operating current decreased to very low values, implying that the device had been triggered into the standby operating mode. However, the only way to recover from this mode was to initiate power cycling, which is not required to recover from a normal standby operating mode. As shown in Figure 3, the cross section for these functional interrupt (SEFI) errors was similar to that of the other two types of functional errors.

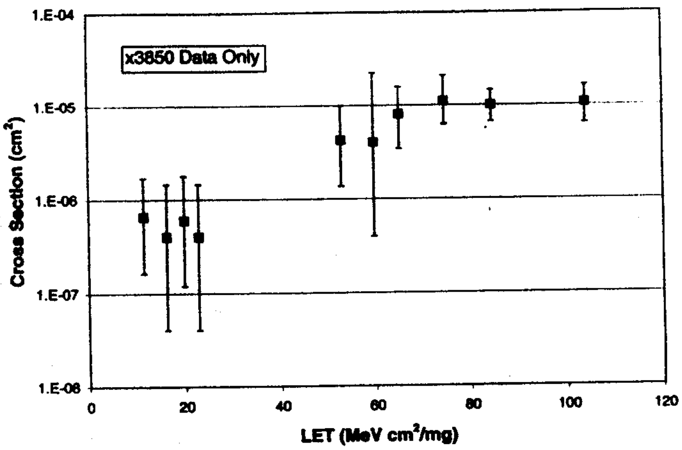

Figure 3. Cross section for "SEFI" events which resulted in loss of output functionality and low operating currents.

Table 2 summarizes the three types of functional errors that occurred, along with the required sequence to recover from the erroneous condition. The devices always recovered completely provided the proper recovery method was used. None of the errors affected the internal programmed state of the PROM.

Table 2. Functional Errors Observed During SEU Tests of the XQ1701L PROM

Error Type	Circuit Effect	Recovery Method
EOP	False EOP signal; output lockout	Reset or power cycle
Address	Address error	Reset or power cycle
SEFI	Stuck output condition; low operating current	Power cycle only

Latchup Test Results

Latchup test results are shown in Figure 4. The cross section is plotted as a function of effective LET, assuming that the "cosine law" applies. There is reasonable agreement between data points for ions at normal incidence with others at nearly the same LET at angle (note the similarity in cross section for LET = 84.6, iodine at 0 °; and LET = 74.7, bromine at 60 °), implying that the cosine law assumption is valid for this device. The effective ranges of the two ions are 18 and 30 µm, respectively without considering the thickness of passivation or metal layers.

The threshold LET for latchup is approximately 55 MeV-cm2/mg, as determined from the null results at LET = 52.8 and the general shape of the LET cross section. Latchup results for the unprogrammed device (x3848) under static bias were consistent with dynamic results obtained for the other two samples.

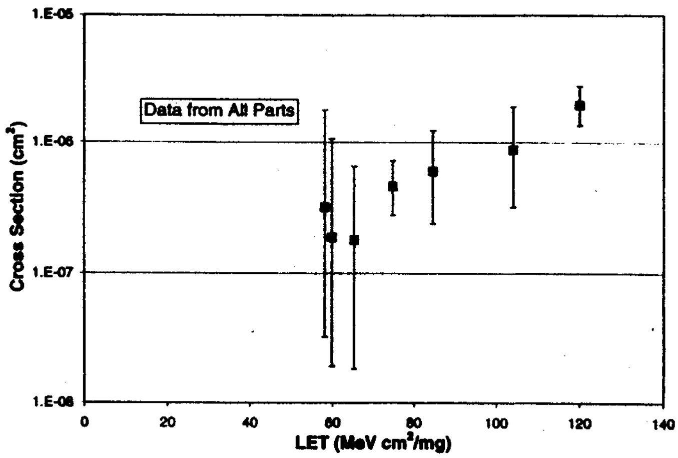

Figure 4. Cross section for latchup in the XQ1701L PROM.

During latchup testing, the higher than normal operating current was detected and measured within about 100 ms. After 500 ms, power was temporarily removed. Latchup equilibrium voltages -- that is, the voltage reached by the device during latchup with the current limited to 20 mA -- were measured for each latchup event. A histogram of these voltages is shown in Figure 5. The voltage distribution for the majority of latchups ranged from 2 to 3 V, but two latchup events were observed with significantly higher voltages. These results will be discussed in more detail in the complete paper.

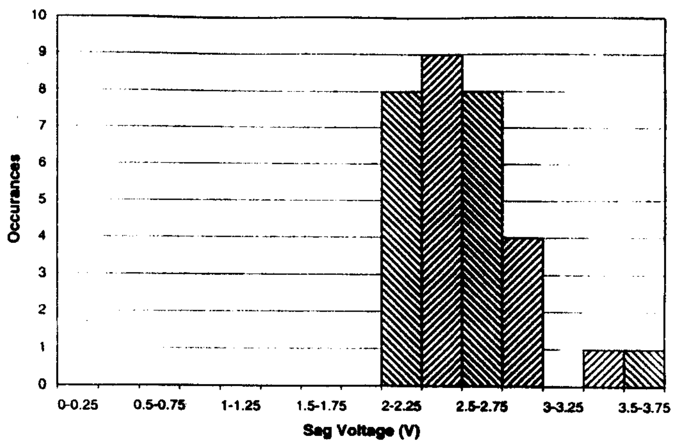

Figure 5. Histogram of equilibrium voltages that occurred just after latchup in the XQ1701L PROM.

Discussion

Four different failure modes were observed during SEU tests of the XQ1701L PROM device. These included three functional operational modes: (1) end-of-program errors; (2) address failures; and (3) stuck-bit failures. The first two types of errors could be recovered from by applying a reset signal to the device, but the third type of error could only be recovered from by cycling the power.

All three types of functional errors had similar threshold LET values and cross sections. The estimated error rate from these types of upsets is about 1% per year from galactic rays in space, with a comparable rate per day for an intense solar flare. However, those error rates do not consider the possibility of upset from protons. Proton testing was not done, but other devices on bulk substrates have been sensitive to proton upset when the LET threshold was below approximately 7 MeV-cm^2/mg.

The PROM was also susceptible to latchup, but only at relatively high LET (55 MeV-cm^2/mg). Because of the high threshold LET, the probability of latchup is relatively low in these devices, and the risk is probably acceptable for many applications.

One way to mitigate SEU effects in these devices is to control the time period during which they operate. Since they are only used to initialize FPGA devices during start-up periods, it is relatively straightforward to minimize the time which they actually operate. An alternative approach is to cycle the power in the PROM just before configuring or reconfiguring the FPGA devices that are driven by the PROM to avoid the functionality errors that can be induced by SEU effects. However, this is less desirable because latchup, if it occurs, would continue for extensive periods until the next power cycle occurs. Either approach precludes reliable, continuous comparison of the FPGA configuration with the PROM.

SEE effects in the XQ1701L do not preclude its use in space, but system users must assure that the functional errors caused by heavy ions do not cause catastrophic system effects. Although proton testing was not done, the low threshold LET makes it likely that protons will cause all three upset phenomena in the PROM to occur. This will increase the estimated error rates, particularly in earth-orbiting systems that have to pass through the earth's proton belts. Alternatively users may wish to wait for Xilinx to release the 7μm epi replacement PROM currently under development and expected to have better latchup performance [7].

References

1. R. Katz, et al. "SEU Hardening of FPGAs for Space Applications and Device Characterization," IEEE Trans. Nucl. Sci., 41, 2179 (1994).
2. G. M. Swift and R. Katz, "An Experimental Survey of Heavy-Ion Induced Gate Rupture in Actel Field Programmable Gate Arrays, RADECS95 Proceedings, IEEE Special Publication 95TH8147, p. 425.
3. R. Katz, et al., "Radiation Effects on Current Field Programmable Elements," IEEE Trans. Nucl. Sci., 44, 1945 (1997).
4. G. Lum and G. Vandenboom, "Single Event Effects Testing of Xilinx FPGAs," 1998 MAAPLD Conference.
5. J. J. Wang, et al., "Actel Antifuse FPGA for Space Applications," , p. 11, Workshop Record from the 1997 RADECS Conference, Cannes, France, September, 1997.
6. R. Katz, et al., "Current Radiation Issues for Programmable Elements and Devices, IEEE Trans. Nucl. Sci., 45, 2600, 1998.
7. Howard Bogrow, Xilinx Engineer, personal communication.